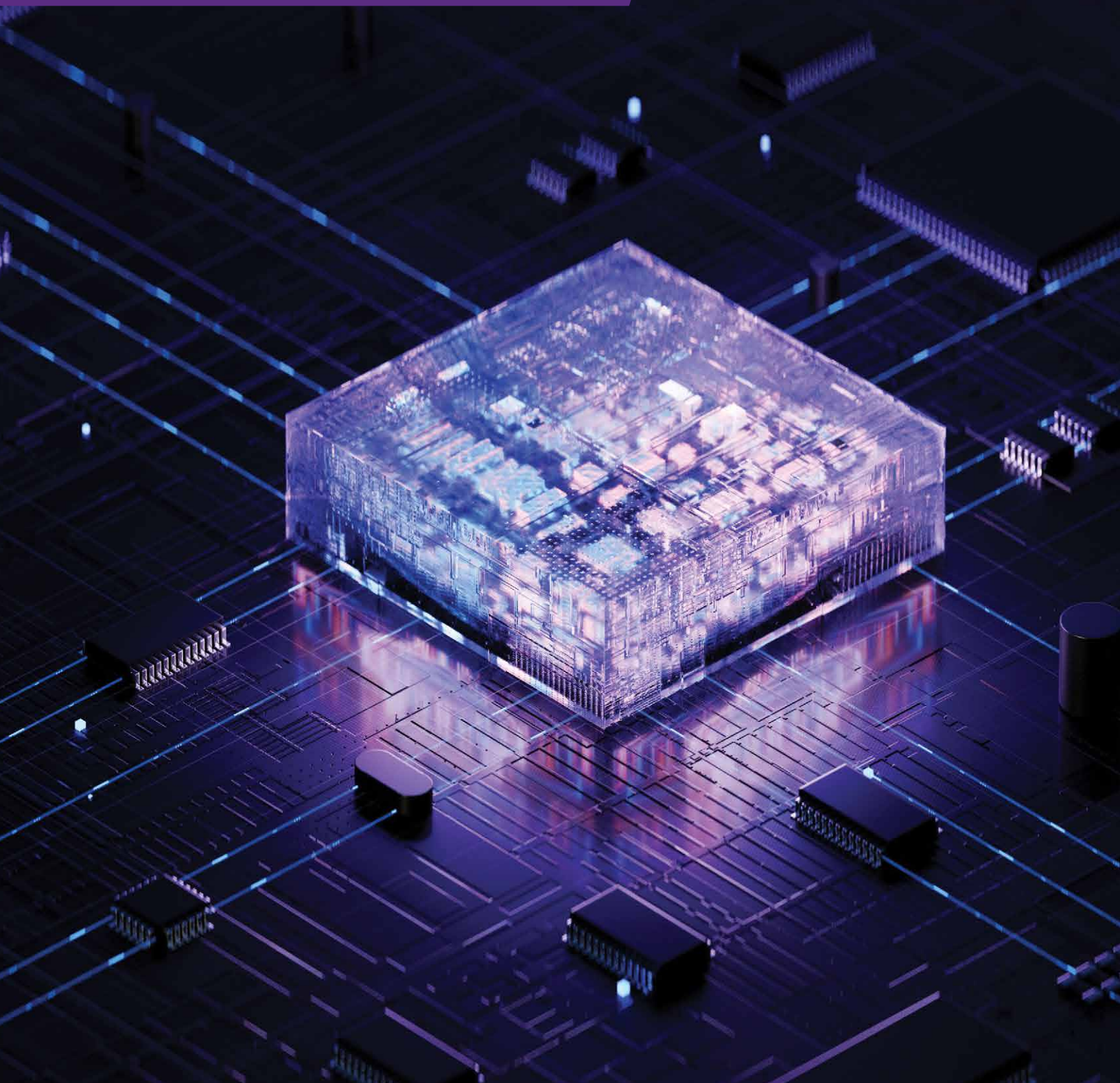
SYNOPSYS®

IP Accelerated

Synopsys IP Subsystems, Tuned to Your SoC



Overview

In the past, only a few top semiconductor companies with big design teams and deep market expertise could create advanced system-on-chip (SoC) designs. Now, the demand for these advanced chip designs is greater than these companies can handle, partly due to the lack of skilled engineers with specialized expertise. Additionally, systems companies are facing the dual challenges of creating their own specialized chips to stay competitive and global trade uncertainties, which push them to build their own SoC design skills.
The growing need for new chip designs in areas like AI/ML, HPC data centers, edge computing, wireless networks, and cars highlights the importance of experienced designers who can quickly and reliably create advanced SoC designs, integrate complex semiconductor IP, build customized IP subsystems, and keep quality high, timelines short, and risks low.

Comprehensive IP Subsystem Solutions for a Competitive Edge

Building and integrating today's complex IP subsystems requires combining IP expertise, application knowledge, and SoC implementation skills. The Synopsys IP Accelerated initiative delivers advanced interface IP subsystems for implementation in cutting-edge process technology nodes from leading semiconductor foundries. We partner closely with our customers to maximize IP integration, IP subsystem hardening, and signal and power integrity results to meet precise SoC design goals through:

Subsystem Feature Selection: Customizing protocol options, functional safety, reliability, security, latency, and performance.

IP Configuration and Subsystem Architecture: Tailoring bus widths, lanes, bifurcation, buffer sizing, and built-in self-test (BIST) mechanisms.

Physical Implementation: Designing optimal floorplans and bump maps to maximize beachfront area, power efficiency, and overall performance.

Package, Signal/Power Integrity: Enhancing power delivery networks, on-die decoupling capacitors, and package/channel analysis for robust signal and power integrity.

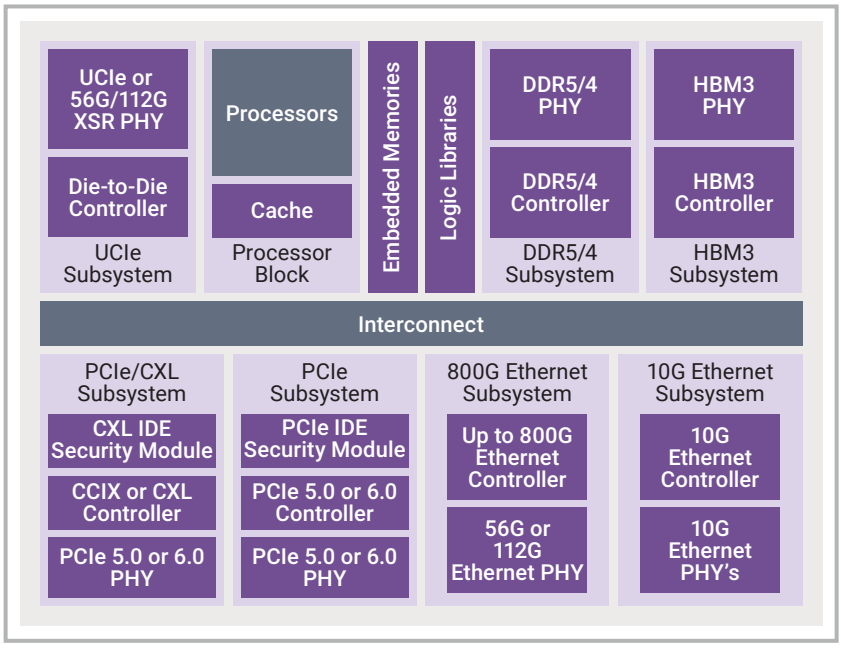


Figure 1: IP Accelerated SoC Subsystem Solutions

> *"The Synopsys team made detailed recommendations to test and bring up our AI SoC's complex interfaces, helping ensure our on-schedule launch."*
>
> ~R&D Director, Leading Artificial Intelligence Computing Company

Accelerate SoC Development and Enhance Design Success

Leveraging extensive experience in HPC, AI, networking, mobile, and automotive applications, Synopsys' IP Accelerated initiative significantly reduces development time and increases the first-pass silicon success rate of SoC designs. This comprehensive approach helps market leaders to swiftly bring innovative products to market, maintaining their competitive edge in a rapidly evolving landscape.

IP Subsystem Solutions

Synopsys' pre-verified, customizable Interface IP subsystems are available for a wide range of Interface IP applications optimized to maximize performance, reduce power consumption, and accelerate time-to-market. Systems are fully integrated IP controllers and IP PHYs consisting of a soft PCS block and multiple pre-hardened elements, in addition to custom logic for testability and verification. Each IP block is configured per the customer's application requirements.

Benefits of Synopsys IP Subsystems

1. Leverage Synopsys IP and SoC experts to configure and deliver IP subsystems tailored to the design requirements.
2. Customized IP subsystems are delivered within weeks for seamless integration into SoC.
3. Collaborative, communicative process frees design teams to focus on product differentiation.
4. First-time-right integration of complex IP subsystems speeds time-to-market.

The IP subsystems come with a comprehensive verification test bench environment consisting of end-to-end test suits using Synopsys Verification IP (VIP) and scoreboard checkers. Each IP subsystem is rigorously verified for functional correctness and adherence to design requirements and industry standards for seamless integration into the SoC. Synopsys IP Subsystems enable designers to streamline their development process, reduce time-to-market and development risk, and increase the quality of the final SoC. Equipped with fully verified IP subsystems, designers can focus on their core competencies while adopting the latest generation of interconnect protocols and scale with new workloads.

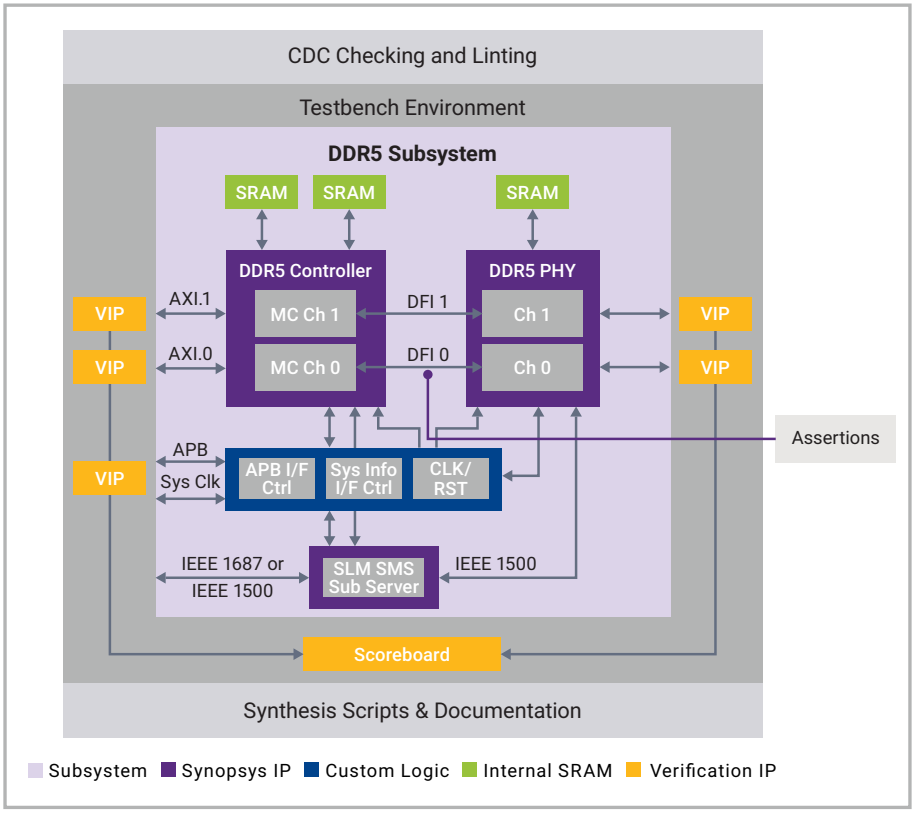


Figure 2: DDR Subsystem Example with Verification Test Bench

IP Subsystem Hardening

Each SoC's performance, floorplan, bump map, and beachfront requirements are unique, requiring a customizable IP subsystem that meet the specific requirements. Optimizing the subsystem implementation to meet the design targets and requirements involves analyzing and fine tuning the design parameters and implementation flow. When it comes to SoC digital design implementation, each step in the RTL-to GDSII process is highly compute intensive – evaluating various floor plans to minimize latency and maximize efficiency, automating placement, implementing the IP subsystem into the chip, and completing signoff. Synopsys IP Subsystem Hardening solutions offer extensive RTL-to-GDSII design expertise, drawing on Synopsys' long experience of delivering hundreds of hardened IP subsystems using Synopsys' high-speed DDR, HBM, PCIe, Ethernet, and SerDes Interface IP. For high-performance designs, Synopsys IP Subsystem hardening enables:

- Faster Synopsys PHY IP subsystem hardening and time-to-market.
- Floorplan exploration to find the optimal solution for a given PHY IP subsystem and SoC.
- Area and power optimization, in line with the chip's system design and performance requirements.
- Custom hardening layout for higher performance.
- Use of Synopsys GPU acceleration tool flow and data center processing power.

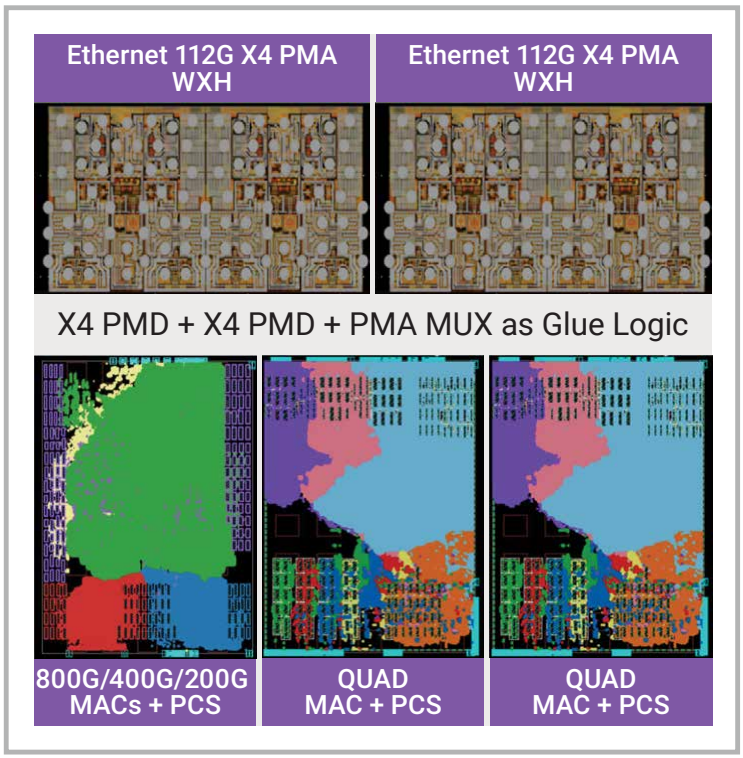


Figure 3: Ethernet Multi-Link Subsystem Floorplan N/S Orientation

Signal Integrity and Power Integrity Solutions

For successful high-performance interfaces, designers need a well-controlled signal integrity and power integrity (SIPI) environments during the design and layout phase. Synopsys supports designers in creating such environments with tight skew control, optimum termination values, and clean reference levels, helping to ensure signal and power integrity compliance in today's high-speed designs. Synopsys SIPI environments:

- Help ensure proper system interface function, features, and timing with verified signal and power integrity.
- Optimize cost/performance between evaluation and production systems.
- Provide system signal and power integrity trade-off analysis on die/package/PCB to optimize cost/performance.
- Offer thorough signal and power integrity analysis to help ensure first-pass silicon and system operation success.
- Expedite system bring-up -determined RX/TX settings.

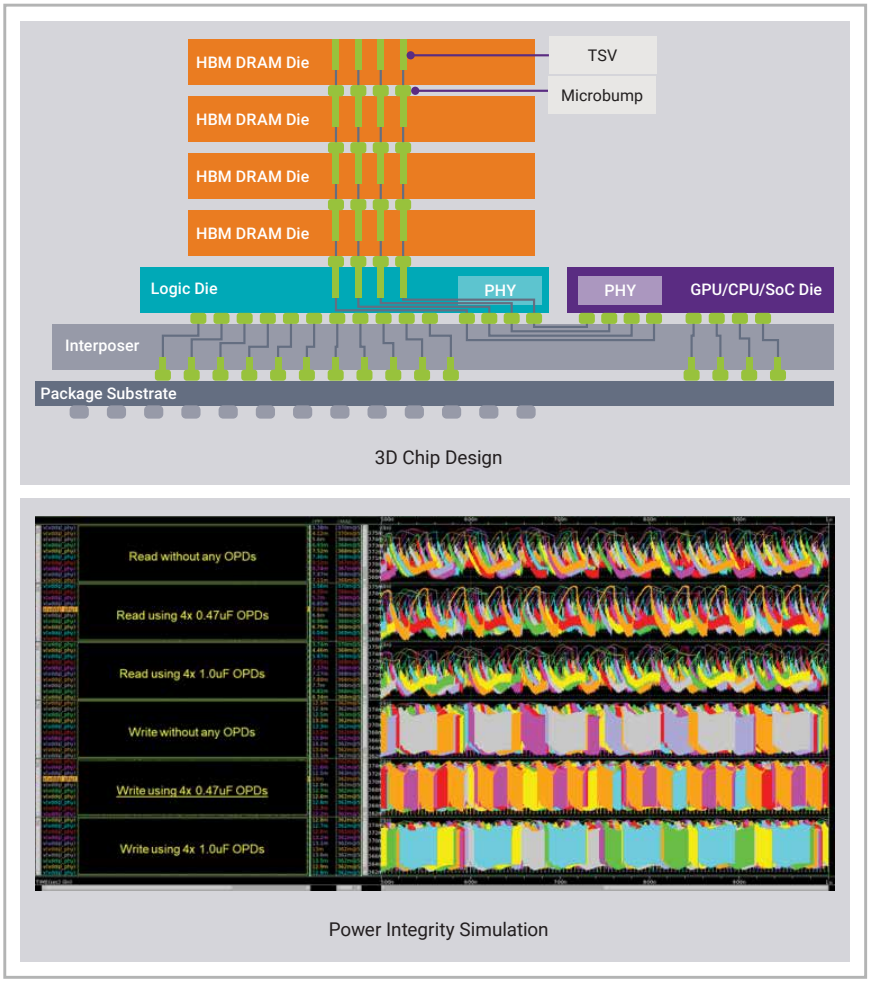


Figure 4: Floorplan & Power Integrity Power Distribution Network Analysis

> *"The combined hardening and SIPI consultation resulted in a gain of +32ps martin across the LPDDR4-3200 interface, and using the IP subsystem accelerated our overall design cycle."*
>
> ~ASIC Design Director, Leading Mixed-Signal Semiconductor Company

Interface IP Silicon Bring-Up Solutions

Every SoC design project has unique requirements, and the IP test plan needs to align with its goals. Synopsys Silicon Bring-Up Solution helps designers prepare, execute and track progress of the interface IP subsystem bring-up plan. During the process, Synopsys experts share their in-depth knowledge of the IP, either remotely or with on-site, worldwide support.

Silicon bring-up solutions accelerate and reduces risk in successful and on-time SoC bring-up with broad expertise to speed crucial IP function validation.

Synopsys IP Accelerated

As the demand for advanced SoCs increases, particularly for applications like artificial intelligence, high performance computing, mobile, and autonomous vehicles, SoC design teams are required to integrate pre-verified, high quality and low risk IP subsystems. Providing customers with a complete IP subsystem solution simplifies SoC integration, optimizes performance, and helps mitigate risks. Synopsys' IP Accelerated Initiative has a proven track record of helping SoC designers integrate advanced IP subsystems with high performance in a timely manner. Designers worldwide trust Synopsys to deliver application-specific IP subsystems in advanced technology nodes, enabling them to get to market faster and without compromise.

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, interface IP, security IP, embedded processors, and subsystems. To accelerate IP integration and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.

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